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APPLICATION	NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/822,997		04/13/2004	Jean-Marc Dortu	INFN/0080	4665	
46798	7590	10/03/2005		EXAM	EXAMINER	
PATTERSON & SHERIDAN, LLP				TRAN, ANDREW Q		
3040 POST OAK BLVD., SUITE 1500				ART UNIT	PAPER NUMBER	
	HOUSTON, TX 77056			2824		
				DATE MAILED: 10/03/2005		

Please find below and/or attached an Office communication concerning this application or proceeding.

Application No.	Applicant(s)					
10/822,997	DORTU ET AL.					
Examiner	Art Unit					
	2824					
ars on the cover sheet with the c	orrespondence address					
IS SET TO EXPIRE 3 MONTH(TE OF THIS COMMUNICATION (a). In no event, however, may a reply be time apply and will expire SIX (6) MONTHS from ause the application to become ABANDONE late of this communication, even if timely filed	N. nely filed the mailing date of this communication. D (35 U.S.C. § 133).					
Responsive to communication(s) filed on This action is FINAL . 2b)⊠ This action is non-final.						
Since this application is in condition for allowance except for formal matters, prosecution as to the merits is						
parte Quayle, 1935 C.D. 11, 45	53 O.G. 213.					
9)⊠ The specification is objected to by the Examiner. 10)⊠ The drawing(s) filed on <u>13 April 2004</u> is/are: a)⊠ accepted or b)□ objected to by the Examiner.						
awing(s) be held in abeyance. See	e 37 CFR 1.85(a).					
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miner. Note the attached Office	Action or form PTO-152.					
have been received in Application have been received y documents have been received	on No ed in this National Stage					
4) Interview Summary						
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DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The specification has failed to adequately and sufficiently describe the "control device" (for example in claim 1, line 4) or the "control means" (for example in claim 14, line 4) for performing a destructive read command, a write command, a nondestructive read command, or a refresh command, as recited in the pending claims. A mere simple timing diagram, as depicted in Fig. 2, appears to be an unreasonably sufficient disclosure for such "control device" or "control means" for executing said defined commands, absent an exemplary embodiment.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Numerous claims recite the terms "opening" which appears to be indefinite. Clarification is required. Examples of such recitations are as follows: in claim 1, line 10; in claim 8, line 7; or

in claim 14, line 8. Further in claim 8, line 5 and 7, the terms "the bit line" and "the word line" lack proper antecedent bases. It is suggested to change said terms to read --a bit line-- and --a word line--, respectively. In claim 9, line 2, the phrase "a destructive write command for writing data from" is indefinite because said phrase is unclear in light of the specification. The present specification describes a normal write command at the most.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Vishin (US Pat 6,178,479 hereafter "Vishin"). See the Figs. and col. 3, In. 14-17.

Vishin discloses a memory device comprising a core memory 102 and a cache control 108 for performing a destructive read command as recited in claim 1 (see Fig. 2 and step 208 therein), or a nondestructive read command as recited in claim 3 (see also Fig. 2 and steps 208 and 206). Note further that, as recited in claim 1, the steps performed by the destructive read command of biasing a bit line, biasing a word line, and sensing data stored in a memory cell are all standard steps necessary for a conventional read command. As to claim 2, see Fig. 3. As to claim 4, see Fig. 4. As to claims 5 and 6, see col. 2, ln. 41-67 and further note that SRAM cache 106 is considered a part of Vishin's memory device. As to claim 7, a cache has long been considered and used as a buffer memory.

Claims 8-20 are rejected under substantially similar grounds.

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Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Jinbo et al. (US Pat 5,608,682) describes a semiconductor memory device.

Ji et al. (US Pat 6,801,980) describes a destructive-read random access memory system buffered with destructive-read memory cache.

Maruyama et al. (US Pat 6,879,540) describes a synchronous semiconductor memory device having dynamic memory cells and operating method thereof.

Nong (US Pat 6,885,591) describes a packet buffer circuit and method.

Dortu et al. (WO 2005/008674) describes a semiconductor memory having a short effective word line cycle time and data read-out method thereof.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew Q. Tran whose telephone number is (571) 272-1885. The examiner can normally be reached on Mon - Fri 8:30 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard T. Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Andrew Q Tran Primary Examiner Art Unit 2824

at September 29, 2005